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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,362	12/04/2003	Joseph R. Nicolaisen	016295.1508 (DC-05570)	6951

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,362	NICOLAISEN, JOSEPH R.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,12-14 and 18-20* is/are rejected.

7)☒ Claim(s) *9-11 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1203//04 Dec 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-7, drawn to information handling system, classified in class 361, subclass 780.

   II. Claims 8-13, drawn to a printed circuit board structure, classified in class 174, subclass 255.

   III. Claims 14-20, drawn to a process of making the printed circuit board of Invention II, classified in class 29, subclass 846.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II-III (regarded as a single examinable Group) are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed, in particular, the combination as claimed does not require the dielectric to: 1) have regions of increased permittivity; 2) include a fiberglass mesh foundation and an adhesive material disposed on respective sides of the foundation; and 3) infusing the adhesive material with material having a higher permittivity than the adhesive material. The subcombination has separate utility such as a printed circuit board for use in an electronic application that is not an information handling system.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Applicant's Attorney, Brian Szymczak, on January 04, 2006, a provisional election was made with traverse to prosecute the invention of II-III, Claims 8-20. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-7 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Rejections Based On Prior Art

5. Lee et al. (US 2004/0118600 A1) was relied upon for the rejections hereinbelow.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 8, 12-14 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al.

As to Claim 8, Lee et al. discloses, in Fig. 6, a PCB comprising: a first core 101; a second core 107a; and an insulating material 103 having regions 104a,b of increased permittivity (paragraph [0090], [0092] and [0094]), the insulating material 103 operable to couple the first core 101 to the second core 107a and the regions 104a,b of increased permittivity disposed proximate at least one power plane--comprising "second layer Vcc" and "third layer GND" in Fig. 6--defined between the first and second cores 101 and 107a.

As to Claim 12, Lee et al. further discloses, in Fig. 6: a third core 107b; an additional insulating material 103 having regions 104c,d of increased permittivity (paragraphs [0090], [0092] and [0094]), the additional insulating material 103 operable to couple the first core 101 to the third core 107b and the regions 104c,d of increased permittivity disposed proximate at least one power plane--comprising "fourth layer GND" and "fifth layer Vcc" in Fig. 6--defined by the first core 101 and the second core 107b.

As to Claim 13, Lee et al. further discloses, in Fig. 6, at least two power planes defined between respective cores (i.e., the first Vcc/GND power plane between first core 101 and second core 107a, and the second Vcc/GND power plane between the first core 101 and third core 107b); and at least two regions (regions 104a and 104b in the first power plane and regions 104c and 104d in the second power plane) of increased permittivity disposed substantially within respective first and second power planes, the two regions of increased permittivity having differing capacitance values (paragraph [0099]).

As to Claim 14, Lee et al. discloses, in Fig. 6, a method for manufacturing a PCB having at least a first core 101 and a second core 107a: integrating an insulating material 104a having a first permittivity into at least a portion of a dielectric layer 103 having a second permittivity (paragraphs [0090], [0092] and [0094]); and coupling the first and second cores 101 and 107a together about the dielectric layer 103 such that the insulating material integrated portions 104a of the dielectric layer 103 substantially align with a power delivery plane (electrodes 105a and 102a of the Vcc/GND power delivery plane in Fig. 6) defined by at least a portion of the first and second cores 101 and 107a (paragraph [0099]).

As to Claim 18, Lee et al. further discloses applying dielectric layer 103 onto the electrodes 102a,b,c,d in first core 101 then, after the application of dielectric layer 103 onto electrodes 102a,b,c,d, reprocessing--i.e., photo-etching--dielectric layer 103 to permit addition of an increased permittivity insulating material 104a,b,c,d therein (Figs. 7b and 7c; paragraph [0103]).

As to Claim 19, Lee et al. further discloses maintaining portions of the dielectric layer 103 substantially free from insulating material 104a,b,c,d where such portions of the dielectric layer 103 substantially align with signal pathways--i.e., the microvias 110 of signal layers 108a,b on the PCB surface--of a selected core; i.e., core 107a or core 107b.

As to Claim 20, Lee et al. further discloses coupling a first panel 101 (Fig. 7a) and a second panel 107a (Fig. 7h) together about the dielectric layer 103 such that the insulating material integrated portions 104a,b of the dielectric layer 103 substantially

align with a power delivery plane (Vcc/GND) to be defined by at least a portion of the first and second panels 101 and 107a (Fig. 6).

Allowable Subject Matter

8. Claims 9-11 and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Suzuki et al. (2004/0099364 A1) discloses, in Figs. 8a,b: a first core B5; a second core B6; and an insulating material A3 having regions 10 of increased permittivity (paragraphs [0086], [0182] and [0276]) the insulating material A3 operable to couple the first core B5 to the second core B6 and the regions of increased permittivity disposed proximate electrodes 8c,d which may function as a power plane defined between the first and second cores B5 and B6 (paragraph [0278]), as is old and well-known in the art, wherein the capacitive region so formed functions as a bypass capacitor for decoupling the power line noise (paragraph [0002]).

b) Kabumoto et al. (US 6,707,685 B2) discloses, in Fig. 4, an insulation layer 22d (col.13: 37-40) having a high permittivity region 29 formed therein (col.14: 51-57).

c) McClanahan et al. (US 5,354,599) discloses vias filled with dielectric material 13a, 25 and 27 having permittivity that is different than the permittivity of the respective insulating layer in which the corresponding dielectric via structures are formed (Figs. 1A,B; col.2: SUMMARY; col.7: 65-col.8: 4). The dielectric material may be of high or low permittivity (e.g., Figs. 6A,B; col.6: 39-50; col.7: 65-col.8: 4).

d) Novak (US 6,215,372 B1) discloses, in Figs. 6 and 7, islands 650, 652 (Fig. 6) and 750-760 (Fig. 7) having higher permittivity than the surrounding insulating layer 612 (Fig. 6), 712 (Fig. 7) (col.7: 26-43). The higher permittivity may be achieved by suspending ceramic particles in the insulating layer 612, 712 (col.7: 41-61) or by coating the insulating material 612, 712 (col.7: 62-67).

e) Ninomiya (US 6,480,396 B2) discloses an insulation layer 26 having a dielectric material 61 formed therein, the dielectric material having a higher permittivity than that of the insulation layer 26 (Figs. 12 and 13; col.6: 39-65), thereby lowering the impedance of power plane 23. Ninomiya further discloses a marking paint 31, also having a relatively higher permittivity than that of the insulation layer 26, thereby lowering the impedance of power plane 23 even further (Fig. 13: col.5: 42-44 and col.6: 66-col.7: 4).

f) O'Bryan et al. (US 6,274,224 B1) discloses an insulating layer infused with dielectric particles to form a high permittivity material in a capacitive device (Figs. 1A,B,C; col.4: 11-27 and col.6: 29-46).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
January 06, 2006